REMARKS

Disposition of the Claims

Claims 1-11 are pending as of the present Office Action, which indicates that claims 1-11 are rejected under 35 U.S.C. 102(b) over U.S. Patent No. 5,117,468 to Hino et al ("Hino").

Claim Amendments

Claim 1 has been amended to improve the form thereof. These changes are not necessitated by the prior art, are unrelated to the patentability of the invention over the prior art, and do not introduce any new matter.

35 U.S.C. 102(b) Rejection

The rejection of claims 1-11 under 35 U.S.C. 102(b) over Hino is respectfully traversed based on the following.

Claims 1-5

Claim 1, as amended, recites *inter alia*:

> a plurality of processors processing respective input image data in parallel with each other and outputting respective processed image data; and
>
> an address memory storing address information for each respective image data processed by said plurality of processors.[1]

In accordance with the standard set down by the MPEP for rejecting a claim under 35 U.S.C. 102, "for anticipation under 35 U.S.C. 102, the reference **must teach every aspect** of the claimed invention either explicitly or impliedly."[2] However, as discussed

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[1] Emphasis added.
[2] MPEP 706.02 (8th ed.)(emphasis added).

below, Hino fails to teach at least an address memory as recited in claim 1, and therefore fails to anticipate claim 1.

Hino is directed to an image processing system comprising cascaded shift registers and one or more image processing circuits. The Hino system also includes an input line from which pixels from an original image can sequentially be inputted into the cascaded shift registers. A group of the shift registers are also connected to the image processing circuit(s) such that a predetermined region of pixels is inputted into the image processing circuit(s) each cycle, the region scanning in a predetermined direction relative to the original image.

Hino provides block diagrams of the image processing circuit in Figs. 6 and 7. Basically, the image data to be processed is input through a direct memory access controller (DMAC), which retrieves the image data from memory. The retrieved image data is processed by local image processing circuits and then the processed image data is output through a second DMAC to memory. As shown in Hino, Fig. 2, the Hino system includes an image memory that the image processing circuit retrieves image data from and sends processed image data to. Hino discloses that the second DMAC includes a register 37A that stores a destination address DA for indicating a location in the image memory where the head of processed image data is to be written. However, since the second DMAC handles processed images in succession, the register DA must be updated for each successive processed image to be stored in the image memory. Thus, the register DA only stores one successive address at a time, and is therefore not capable of anticipating the address memory, which stores more than one address information at a time, as recited by claim 1.

The Office Action alleges that Hino also discloses an address memory, citing col. 2, lines 38-46 of Hino. However, this allegation is respectfully traversed. The cited portion of Hino includes a disclosure of a first memory means, which Hino indicates is "for storing therein two-dimensional image data (that is, original image data) to be

processed,"[3] and a second memory means, which Hino indicates is "for storing therein image data which has been subjected to image processing."[4] Thus, each of the first and second memory means disclosed in the cited portion of Hino store image data, not address information as recited in claim 1.

Therefore, since Hino fails to disclose all of the limitations of claim 1, Hino cannot anticipate claim 1, or claims 2-5 which depend from claim 1.

Claims 6-10

Claim 6 recites *inter alia* "a first memory storing arrangement information in original image data for said plurality of divided data." Thus, for Hino to anticipate claim 6, Hino must teach *inter alia* a memory storing arrangement information as recited in claim 6.

As pointed out above, Hino discloses memory storing image data both before and after image processing. However, Hino does not disclose storing arrangement information in memory just as Hino does not disclose storing address information in memory. Also, Hino teaches a processing system that allows the image data to be reconstructed based on the order in which it is output from the processing circuits since the image data is always input in order as the data is scanned from the image. Thus, Hino fails to even suggest anything related to arrangement information for divided image data. Therefore, since Hino fails to disclose all of the limitations of claim 6, Hino cannot anticipate claim 6, or claims 7-10 which depend from claim 6.

Claim 11

Claim 11 recites *inter alia*:

> outputting said processed data as well as address information indicating arrangement of said divided data; and

[3] Hino, col. 2, lines 40-42.
[4] *Id.*, lines 42-44.

restoring a single image from said processed data in accordance with said address information.

Thus, for Hino to anticipate claim 11, Hino must teach *inter alia* the steps of outputting and restoring as recited in claim 11. However, Hino is silent with regard to address information that indicates an arrangement of divided data. Instead, the Hino processor processes the image data in a sequential manner, outputting the image data in a manner that allows the image to be reconstructed based simply on the order in which the image data is output. Thus, Hino fails to disclose or suggest restoring an image in accordance with address information that indicates an arrangement of the divided data. Therefore, since Hino fails to disclose all of the limitations of claim 11, Hino cannot anticipate claim 11

Accordingly, it is respectfully requested that the rejection of claims 1-11 under 35 U.S.C. 102(b) be reconsidered and withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited.

This Amendment does not increase the number of independent claims, does not increase the total number of claims, and does not present any multiple dependency claims. Accordingly, no fee based on the number or type of claims is currently due. However, if a fee, other than the issue fee, is due, please charge this fee to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260.

If an extension of time is required to enable this document to be timely filed and there is no separate Petition for Extension of Time filed herewith, this document is to be construed as also constituting a Petition for Extension of Time Under 37 C.F.R. § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

Any other fee required for such Petition for Extension of Time and any other fee required by this document, other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

Respectfully submitted,

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